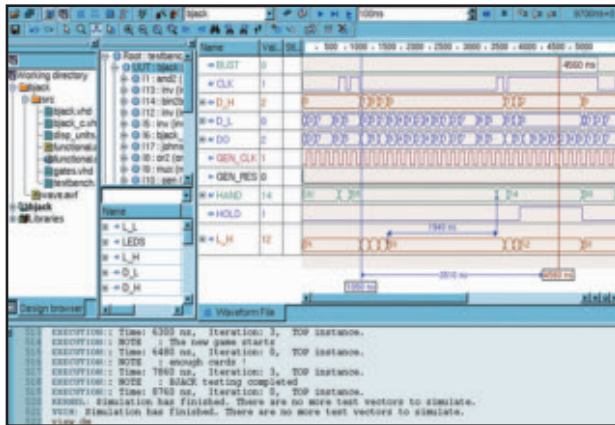


RIVIERA is the ultimate performance-driven ASIC and FPGA design verification solution. This “Best-in-Class” approach results in the most versatile VHDL, Verilog, SystemVerilog, and SystemC mixed-simulation platform available. Riviera is ideal for RTL debugging, long regression testing, timing simulation, and team-based design methodologies including direct connection to hardware acceleration and server farm.



CO-SIMULATION WITH C/C++ AND SYSTEMC™

C/C++/SystemC integrate seamlessly with Riviera. Riviera includes the ability to co-simulate C/C++ and SystemC testbenches to design modules in connection with VHDL, Verilog and SystemVerilog. The RTL simulator connects directly to objects generated by the C/C++ compiler (gcc or Visual Studio).

OPTIMIZED SIMULATION MODES

Riviera can be configured to optimize simulation and increase performance.

- Sophisticated optimization techniques increase simulation speed by giving up some debugging options.
- System Level Platform (SLP) - New acceleration technology for ultra fast simulation of Verilog netlists.
- Sparse Memories - large memory blocks modeled in HDL do not use system memory until the design reads or writes data to such a block (system memory is allocated only for the required address range).

HIGH PERFORMANCE WAVEFORM VIEWER

The Waveform Viewer uses several compression techniques for handling large simulation databases and making the display, scrolling, and zooming instantaneous. In addition to performance, the Waveform Viewer includes features to allow fast and convenient analysis of the simulation data. For example:

- Show Event Source (jumps to the HDL statement that caused the event shown in the waveform)
- Virtual buses
- List View panes with a tabular view of the data
- Graphical waveform comparison
- Command line waveform comparison tool
- Various conversion utilities (e.g. vcd2asdb, asdb2vcd)

ASSERTION-BASED VERIFICATION

Using Assertion-based Verification in Riviera adds value throughout the process of design, integration, system simulation and tape out by providing a better (internal) understanding of the design. Assertions speed debugging by reducing verification iterations, improving design re-use and outsourcing and can also be utilized in hardware (Riviera-IPT). Assertion standard support includes:

- OpenVera Assertions (OVA)
- Property Specific Language (PSL)
- Open Verification Libraries (OVL)
- SystemVerilog Assertions (SVA)

MIXED LANGUAGE SIMULATION

Riviera supports development of complex IC designs consisting of VHDL, Verilog, C/C++, SystemC, SystemVerilog and EDIF Netlist design blocks and provides seamless integration from a common simulation kernel.

IEEE INTERFACES

Riviera includes IEEE standard PLI, VPI and VHPI interfaces for connection to other verification tools in the design flow. In addition to the standard interface, Riviera also includes optimized integration to select strategic partner tools.

SERVER FARM SUPPORT

Riviera is compatible with all server farm load management methodologies configured for UNIX, Linux or Windows operating systems. Designs can be off-loaded from local workstations or a PC to a central location, freeing the local machine to work on other parts of the design.

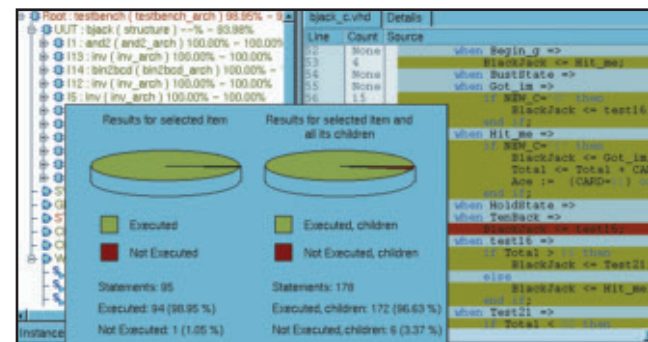
LIBRARY ENCRYPTION

Riviera provides source compression and encryption for VHDL and Verilog to safely pack and distribute designs among team members locally or over a network.

CODE COVERAGE

Coverage tools typically put large overhead on the simulators and slow their run time. Because this feature is built directly the Riviera simulation kernel and does not require any instrumented code, overhead is substantially reduced.

- Line Coverage (per Instance/Unit) / Branch Coverage
- Coverage Viewer
- Coverage Merge
- Toggle Coverage
- Functional Coverage (with PSL, OVA, and SVA)



ADVANCED DEBUGGING TOOLS

Riviera allows entering and debugging of VHDL, Verilog, SystemVerilog and mixed designs. Riviera allows for source code debugging online or post simulation using several advanced features that give designers total control over the source code while speeding design debugging.

MEMORY VIEWER

Riviera simplifies debugging by displaying the content of memories defined in a design for both VHDL and Verilog. The values stored can be observed and modified during simulation.

SIGNAL AGENT (VHDL ONLY)

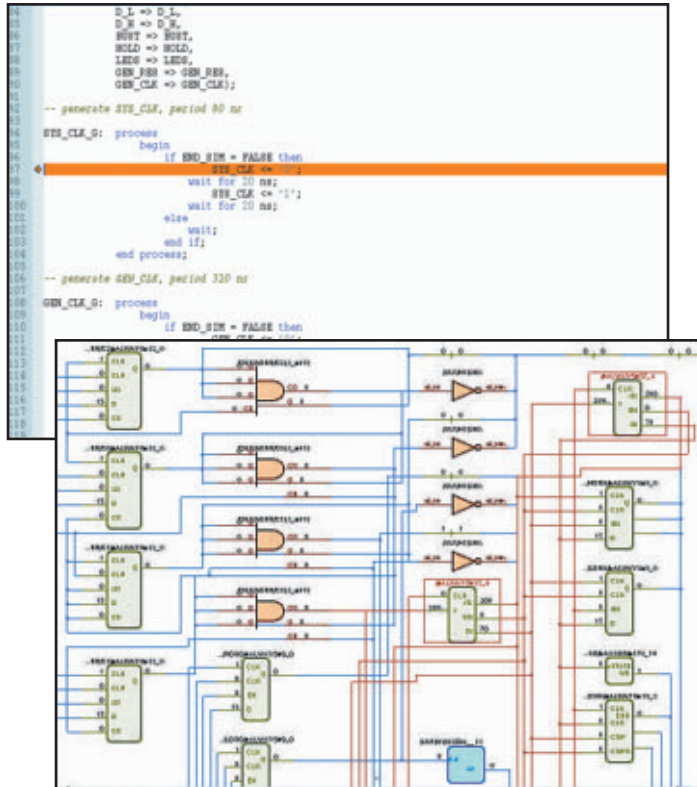
Signal Agent allows a designer to monitor and drive signals from any VHDL block. Signals do not have to be routed via the interface or declared in global packages. This is particularly useful in testbench development and design verification.

X-TRACE

X-Trace allows the designer to trace and view events that cause unexpected output values during simulation. It is accessed through the Advanced Dataflow window in conjunction with the Waveform Viewer. Using X-Trace will drastically reduce overall debug time.

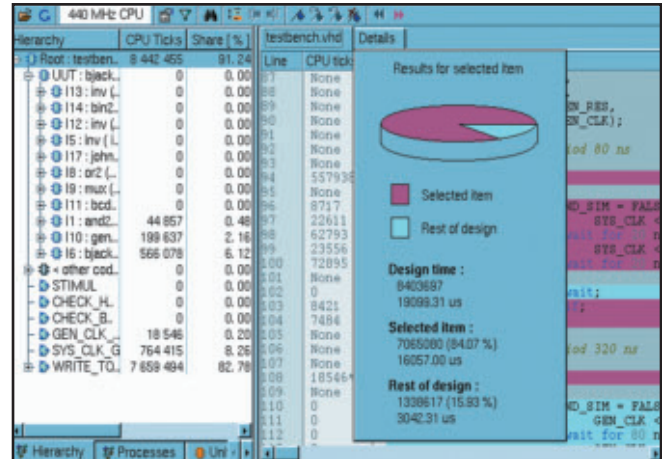
ADVANCED DATAFLOW

Advanced Dataflow offers the ability to view and debug the design graphically. It is useful for exploring the physical connectivity of the design for both VHDL and Verilog. Advanced Dataflow connects directly to Riviera's stand-alone Waveform Viewer using the cursor to scroll back and forth through simulation while observing the annotated values in the diagram.



DESIGN PROFILER

Design blocks that consume more simulation runtime can be easily identified using the Design Profiler. By identifying these blocks and focusing on these areas the overall design simulation time can be significantly decreased. Without the ability to see the design characteristics and identify simulation degradation, simulation can be highly inefficient.



RIVIERA-IPT HARDWARE ACCELERATION

Riviera can be upgraded with an optional patented hardware accelerator, Riviera-IPT, which provides greater speed and efficiency by bringing together many different design and verification elements on one seamless, accelerated system-level platform. This platform combines software simulation for mixed VHDL and Verilog with C/C++ / SystemC co-simulation and hardware acceleration, all optimized and connected to a common kernel architecture. Key features include:

- 10X + RTL Acceleration
- No Learning Curve or Set-up Time
- Higher Design Quality
- Scalable Architecture
- Network and Team-Based Operation

RIVIERA-IPT METHODOLOGY

Traditional simulation methodologies require users to re-simulate previously proven HDL blocks with each newly added block or design iteration, making verification slow and inefficient. However, since Incremental Prototyping Technology "pushes" all verified blocks into hardware, Riviera-IPT only simulates the newly added HDL blocks in software, dramatically accelerating the simulation process.

PRODUCT SUPPORT

Aldec provides the highest level of customer support in the industry. Annual product maintenance includes unlimited technical support around the globe, quarterly product releases and updates, subscription to our newsletter and newsgroups including access to our on-line support library.

RIVIERA FEATURES

OS Platforms Supported

- Sun Solaris
- Linux
- Windows NT/2000/XP

System Requirements


- Sparc or Pentium PC Compatible Computer
- Hard Disk Drive with 300MB of Free Space for Windows
- Hard Disk Drive with 410MB of Free Space for Unix
- Hard Disk Drive with 470MB for Linux 32bit
- Hard Disk Drive with 430MB for Linux 64bit

Standards Support

- VHDL 1076-87/93
- Verilog 1364-95/2001
- VITAL 1076.4-95/2000
- SDF 1.0, 2.0 and 3.0
- SystemVerilog 3.1a
- SystemC 2.1
- EDIF 2.0.0

Interface

- TCL/TK
- PERL
- SWIFT
- PLI / VPI
- VHPI
- C++



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Supported Languages	Riviera	Riviera-PRO
VHDL	•	•
Verilog® HDL	•	•
SystemC™	•	•
EDIF 2 0 0	•	•
SystemVerilog 3.1a (Design)	•	•
SystemVerilog 3.1a (Assertions)		•
PSL (Assertions)		•
OVA (Assertions)		•
Simulation		
Common Kernel Simulator	•	•
Mixed VHDL/Verilog/SystemC/SystemVerilog Simulation	•	•
Optimized Verilog Netlist Simulation (SLP Technology)	Optional	Optional
Verilog Incremental Compilation	•	•
Verilog Programming Interfaces (PLI/VPI)	•	•
VHDL Programming Language Interface (VHPI)	•	•
Value Change Dump (VCD and Extended VCD) Support	•	•
Platform Independent Libraries	•	•
Simulation Model Protection/Library Encryption	•	•
Library Refresh	•	•
Simulation Save and Restore	•	•
Support for 64-bit Simulation Engine		•
Debug and Analysis		
Interactive Code Execution Tracing	•	•
Advanced Breakpoint Management	•	•
Accelerated Waveform and List Viewer	•	•
Waveform Compare	•	•
Multiple Structure Browsers and Waveform Windows	•	•
Memory View	•	•
Watch Window	•	•
Call Stack	•	•
C Debugger	•	•
Processes View	•	•
Advanced Dataflow	•	•
XTrace	•	•
Profiler (Performance Metrics)	•	•
Hierarchical References to/from VHDL (Signal Agent)	•	•
Assertion Viewer		•
Verilog and/or VHDL Lint		•
External Simulation Interfaces		
Synopsys SmartModels®, SWIFT™ Interface and LMTV	•	•
Novas FSDB Writer	•	•
Denali Memory Model Interface	•	•
Cadence Specman Elite Interface	•	•
Co-simulation Support		
MATLAB® Co-simulation	•	•
Simulink® Co-simulation	•	•
Coverage Tools		
Statement and Branch Coverage	•	•
Toggle Coverage	•	•
Assertion Based Functional Coverage		•
Working Modes		
GUI Mode	•	•
Command Line Mode	•	•
Batch Mode	•	•
Design Entry and Design Management		
HDL and Text Editor	•	•
Language Assistant with Templates and Auto-complete	•	•
Design Manager	•	•
Tcl Scripting and Macro Language	•	•
Operating Systems Support		
32-bit Operating Systems	Linux, Solaris, Windows® XP/2000/NT	
64-bit Operating Systems	Linux (x86_64)	